PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Louis A. Lippincott Examiner: Duy Dang

Serial No.: 10/600,047 Group Art Unit: 2624

Filed: June 19, 2003 Docket: 884.898US1

For: PROCESSOR TO PROCESSOR COMMUNICATION IN A DATA DRIVEN ARCHITECTURE

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on August 20, 2008, from the Final Rejection of claims 1-6, 9, and 19-30 of the above-identified application, as set forth in the Final Office Action mailed on February 29, 2008.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $540.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

A Notice of Appeal was filed on October 17, 2008 in the following related Application: Serial No. 10/600,048 "Communication Ports in a Data Driven Architecture", Applicant – Louis A. Lippincott, filed on June 19, 2003

3. STATUS OF THE CLAIMS

The present application was filed on July 19, 2003 with 30 claims. In response to a Restriction Requirement mailed on January 16, 2007, an Amendment was filed to cancel claims 10-18. In response to the Office Action mailed on May 21, 2007, an Amendment was filed to amend claims 1, 5, 19, 22, 25-30 and to cancel claim 7. Claims 1-6, 8-9 and 19-30 stand rejected, remain pending, and are subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated February 20, 2008.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to, methods, systems and apparatus for processor to processor communication in a data driven architecture. In claim 1, an apparatus includes a first processor. See Fig. 1 – processor 202A and page 7, lines 5-16. The first processor includes a first processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The apparatus also includes a second processor. See Fig. 1 – processor 202C and page 7, lines 5-16. The second processor includes a second processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The first processor is configured to transmit data to the second processor through a third processor. See Fig. 10, processor 202A, processor 202C and processor 202B, respectively, and page 22, line 1 – page 27, line 15. No processor element within the third processor is configured to perform a process operation on the data as part of the transmission of the data from the first processor to the second processor. See Fig. 3 – processor element 306, page 7, line 26 – page 8, line 11 and page 11, line 11 – page 12, line 27. The first processor includes a type of hardware accelerator that is not included in the second processor. See Fig. 3 – processor elements 306 and page 12, lines 8-19.

In claim 5, an apparatus includes a first processor. See Fig. 1 – processor 202A and page 7, lines 5-16. The first processor includes a first processor element that is configured to perform a first data process operation. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The apparatus also includes a second processor. See Fig. 1 – processor 202C and page 7, lines 5-16. The second processor includes a second processor element that is configured to perform a second data process operation based on an output from the first data process operation. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The first processor is to transmit the output from the first data process operation to the second processor based on a logical connection that includes traversal through a port ring of a third processor. See Fig. 10, processor 202A, processor 202C and processor 202B, respectively, and page 22, line 1 – page 27, line 15. A third processor element within the third processor is not configured to perform a data process operation between the first data process operation and the second data process operation. See Fig. 3 – processor element 306, page 7, line 26 – page 8, line 11 and page 11, line

11 – page 12, line 27. The first processor includes a type of hardware accelerator that is not included in the second processor. See Fig. 3 – processor elements 306 and page 12, lines 8-19. The first processor element in the first processor is configured to perform the first data process operation on data streams received into the expansion interface at least simultaneously in part with second data process operation performed by the second processor element in the second processor. See Fig. 10 and page 22, line 22 – page 23, line 7.

In claim 19, a method includes receiving a stream of data in a first processor having a first processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The method also includes performing, by the first processor element, image processing operations on at least a part of the stream of data. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The method also includes transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The first processor includes a type of hardware accelerator that is not included in the second processor. See Fig. 3 – processor elements 306 and page 12, lines 8-19.

In claim 22, a method includes performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The method also includes executing, by a first processor element in the first image signal processor, an image process operation on the image data. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The method also includes transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-processor point-to-point configuration. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27,

line 15. A type of the hardware accelerator is not included in at least one of the number of other different image signal processors. See Fig. 3 – processor elements 306 and page 12, lines 8-19.

In claim 25, a machine-readable storage medium provides instructions, which when executed by a machine, cause said machine to perform operations. See page 4, lines 1-20. The operations include receiving a stream of data in a first processor having a first processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27. The operations also include performing, by the first processor element, image processing operations on at least a part of the stream of data. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The operations also include transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The first processor includes a type of hardware accelerator that is not included in the second processor. See Fig. 3 – processor elements 306 and page 12, lines 8-19.

In claim 28, a machine-readable storage medium provides instructions, which when executed by a machine, cause said machine to perform operations. See page 4, lines 1-20. The operations include recursively performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The operations also include executing, by a first processor element in the first image signal processor, an image process operation on the image data. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27, line 15. The operations also include transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-processor point-to-point configuration. See Fig. 3 – processor element 306 and page 11, line 11 – page 12, line 27 and Fig. 10 and page 22, line 1 to page 27,

line 15. A type of the hardware accelerator is not included in at least one of the number of other different image signal processors. See Fig. 3 – processor elements 306 and page 12, lines 8-19.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to each of the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-6, 8 and 19-30 were rejected under 35 U.S.C. § 102(b) as being anticipated by Li (EP 0257581A2) (hereinafter Li).

7. ARGUMENT

A) The Applicable Law under 35 U.S.C. §102(b)

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

B) Discussion of the rejection of claims 1-6, 8 and 19-30 under 35 U.S.C. § 102(b) as being anticipated by Li (EP 0257581A2) (hereinafter Li).

Claim 1-4

With regard to claim 1, among the differences, claim 1 recites "wherein the first processor includes a type of hardware accelerator that is not included in the second processor. In Response to Amendment section, the Office indicated that this limitation was disclosed by Li:

> For example, figure 14 in together with lines 26-30 and 5 1-56 of page 7 in Li corresponds to this claimed limitation. In Li, the "square" depicted in figure 14 as described at lines 50-56 of page 6 represents processor element which performs processing operations such as arithmetic operation, logical operation, transform operation according to lines 26-30 of page 6. Such operation described in Li corresponds to claimed "hardware accelerator" according to item 6 (ALU) of figure 1, line 3 of page 7 (hardware ALU), item 96 (ALU) of figure 21. Furthermore, the "circle" depicted in figure 14 represents a pass-through processing element. Therefore, processing element depicted as "square" includes a type of hardware accelerator that is not included in processing

> element depicted as "circle" because processing element depicted as "circle" is programmed as "no-op" or "passthrough".

Office Action at pages 2-3.

Accordingly, the Office is alleging that a shape in figure 14 and associated description is indicative of whether the processing element includes a hardware accelerator or is only a pass-through processing element that does not include a hardware accelerator. In particular, according to the Office, if the shape of the processing element is shown as a square, there is a hardware accelerator and if the shape of the processing element is shown as a circle, there is no hardware accelerator therein. Applicant respectfully traverses. In contrast to what the Office is alleging, Li illustrates that the different processing elements have the same configuration. In particular, figure 1B of Li shows the internal configuration of the different processing elements. Li does not disclose that the processing elements have different configurations. In the description of Li, the processing element is described as follows:

> Processing element 5 is shown expanded to provide drawing space for internal organs ALU 6, MEM 7 and CCM 8 and NESW connections. Overall programming control and housekeeping control is by host computer 3, via bus 9.

Li at page 5, lines 15-16.

Li does not disclose that there are different internal configurations for different processing elements. The processing elements in Li have the same hardware but operate differently depending on how the elements are programmed:

> Note that each PE (processing element) can perform both the pass-through function and a processing operation, as programmed.

Li at page 6, lines 54-55.

Therefore, Li does not disclose that one processor includes a hardware accelerator that is not included in the second processor. Because Li does not disclose each element of claim 1, Applicant respectfully submits that the rejection of claim 1 under 35 U.S.C. §102 has been overcome. Because the claims that depend from claim 1 depend from and further define claim 1,

Applicant respectfully submits that the rejection of the dependent claims under 35 U.S.C. §102 has been overcome.

Claim 5, 6 and 8

With regard to claim 5, among the differences, claim 5 recites "wherein the first processor includes a type of hardware accelerator that is not included in the second processor." Based on the remarks set forth above, Applicant respectfully submits that claim 5 is patentable over Li.

In addition to the remarks set forth above regarding claim 1, Applicant has submits the following. Among the differences, claim 5 recites "wherein the first processor element in the first processor is configured to perform the first data process operation on data streams received into the expansion interface at least simultaneously in part with second data process operation performed by the second processor element in the second processor." The Office indicated that this limitation is disclosed by Li:

> Li does teach that the first processor element in the first processor is configured to perform the first data process operation on data streams received into the expansion interface at least simultaneously in part with second data process operation performed by the second processor element in the second processor, see figure 14 and examiner's response set forth at (i) above. For example, "square" processing element perform data operations (i.e., arithmetic operation, logical operation, transform operation) on the received data streams while "circle" processing element perform "pass-through operation which corresponds to the so called "second data processing oration performed by the second processor element in the second processor".

Office Action at pages 3-4.

Applicant respectfully traverses. None of the cited sections of Li disclose the output from one processor is to be processed, at least simultaneously in part, by a second processor.

Because Li does not disclose each element of claim 5, Applicant respectfully submits that the rejection of claim 5 under 35 U.S.C. §102 has been overcome. Because the claims that depend from claim 5 depend from and further define claim 5, Applicant respectfully submits that the rejection of the dependent claims under 35 U.S.C. §102 has been overcome.

Claims 19-30

Claims 19-30 (as amended) include limitations that are similar to claim 1. In light of the remarks regarding claim 1, Applicant respectfully submits that Li does not disclose each element of claims 19-30. Accordingly, Applicant respectfully submits that the rejection of claims 19-30 has been overcome.

SUMMARY

It is respectfully submitted that the claims are patentable over the cited art. Reversal of the rejection and allowance of the pending claim are respectfully requested.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402

Date 3-20-09 By

Gregg A. Peacock
Reg. No. 45,001

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 20th day of March 2009.

Name Amy Moriarty

Signature

8. CLAIMS APPENDIX

1. An apparatus comprising:

a first processor that includes a first processor element; and

a second processor that includes a second processor element, wherein the first processor is configured to transmit data to the second processor through a third processor, wherein no processor element within the third processor is configured to perform a process operation on the data as part of the transmission of the data from the first processor to the second processor, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

2. The apparatus of claim 1, wherein the first processor is not directly connected with the second processor.

3. The apparatus of claim 1, wherein no processor element within the third processor is involved in the transmission of data from the first processor to the second processor through the third processor.

4. The apparatus of claim 1, wherein the first processor, the second processor and the third processor are coupled together in a point-to-point configuration.

5. An apparatus comprising:

a first processor that includes a first processor element that is configured to perform a first data process operation; and

a second processor that includes a second processor element that is configured to perform a second data process operation based on an output from the first data process operation, the first processor to transmit the output from the first data process operation to the second processor based on a logical connection that includes traversal through a port ring of a third processor, wherein a third processor element within the third processor is not configured to perform a data

process operation between the first data process operation and the second data process operation, wherein the first processor includes a type of hardware accelerator that is not included in the second processor and wherein the first processor element in the first processor is configured to perform the first data process operation on data streams received into the expansion interface at least simultaneously in part with second data process operation performed by the second processor element in the second processor.

6. The apparatus of claim 5, wherein the first processor, the second processor and the third processor are part of a number of processors that are in a point-to-point configuration.

8. The apparatus of claim 5 further comprising,

an expansion interface to receive data on which the processor element in the first processor is to perform the first data process operation; and

a memory interface unit coupled to a memory that is external to the apparatus, wherein the memory is configured to store an output of the second data process operation.

19. A method comprising:

receiving a stream of data in a first processor having a first processor element;

performing, by the first processor element, image processing operations on at least a part of the stream of data; and

transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

20. The method of claim 19, wherein transmitting the result of the image processing operations to the second processor through the third processor includes transmitting the result of the image processing operations to the second processor through a logical connection that includes transmission through a series of processors including the third processor.

21. The method of claim 19, wherein receiving the stream of data in the first processor having the first processor element includes receiving the stream of data in the first processor having the first processor element at least simultaneously in part with performing, by a second processor element in the second processor, a different image processing operation.

22. A method comprising:

performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete,

executing, by a first processor element in the first image signal processor, an image process operation on the image data; and

transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-processor point-to-point configuration, wherein a type of the hardware accelerator is not included in at least one of the number of other different image signal processors.

23. The method of claim 22, wherein transmitting the result of the image process operation to the second image signal processor includes transmitting the result of the image process operation to the second image signal processor through the logical connection, wherein other processing elements in the other different image signal processors do not process the image data prior to processing by a second processor element in the second image signal processor.

24. The method of claim 22 further comprising receiving the image data from a source that is external to the multi-processor point-to-point configuration.

25. A machine-readable storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

receiving a stream of data in a first processor having a first processor element;

performing, by the first processor element, image processing operations on at least a part of the stream of data; and

transmitting a result of the image processing operations to a second processor through a third processor having a third processor element, independent of image processing operations by the third processor element, wherein the first processor includes a type of hardware accelerator that is not included in the second processor.

26. The machine-readable storage medium of claim 25, wherein transmitting the result of the image processing operations to the second processor through the third processor includes transmitting the result of the image processing operations to the second processor through a logical connection that includes transmission through a series of processors including the third processor.

27. The machine-readable storage medium of claim 25, wherein receiving the stream of data in the first processor having the first processor element includes receiving the stream of data in the first processor having the first processor element at least simultaneously in part with performing, by a second processor element in the second processor, a different image processing operation.

28. A machine-readable storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

recursively performing, by a hardware accelerator in a first image signal processor within a multi-processor point-to-point configuration, the following operations until receipt of image data from an image scanning operation is complete,

executing, by a first processor element in the first image signal processor, an image process operation on the image data; and

transmitting a result of the image process operation to a second image signal processor within the multi-processor point-to-point configuration through a logical connection that includes a number of ports of a number of other different image signal processors within the multi-

processor point-to-point configuration, wherein a type of the hardware accelerator is not included in at least one of the number of other different image signal processors.

29. The machine-readable storage medium of claim 28, wherein transmitting the result of the image process operation to the second image signal processor includes transmitting the result of the image process operation to the second image signal processor through the logical connection, wherein other processing elements in the other different image signal processors do not process the image data prior to processing by a second processor element in the second image signal processor.

30. The machine-readable storage medium of claim 28 further comprising receiving the image data from a source that is external to the multi-processor point-to-point configuration.

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.